ABSTRACT OF THE DISCLOSURE

A method and system provide a stable reference clock for use in a communication system. A phase-locked loop (PLL) receives an input clock signal with potentially unacceptable levels of jitter and wander. The PLL provides a synchronized output clock with significantly reduced jitter and wander. The PLL nominally uses a digital-to-analog converter (DAC) to control a voltage-controlled oscillator (VCO). Applying a loop filter function to the phase difference between the input clock and the output clock generates control values for the DAC. Loop filter adaptation is based on control value averages, which enhances stability and frequency locking performance. Frequency lock detection is based on the consistency of the DAC control values, rather than on a predetermined target value, making the PLL a self-calibrating system. The long-term average of the control value in the locked state may be stored for later use as an initial DAC setting.